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EXAMINER	
SUCH, MATTHEW W	
ART UNIT	**PAPER NUMBER**
2891	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/532,078	UNNO ET AL.	
	Examiner	Art Unit	
	Matthew W. Such	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *5-7 and 19-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10 January 2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, drawn to claims 1-4 and 8-18 in the reply filed on 26 July 2007 is acknowledged. The traversal is on the ground(s) that there is no undue burden to search. This is not found persuasive because the case is was filed under 35 U.S.C. 371 and, as such, was restricted by unity of invention under PCT Rule 13.1 and PCT Rule 13.2. When unity is shown to be lacking between groups of inventions, the Examiner is not required to make a showing of burden to search since the inventions lack corresponding special technical features requiring separate searches. See MPEP § 1850 and 1893.03(d).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the top-gate organic transistor configurations, as described in claims 12-15, for example, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must

be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 8-10 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Kelley ('676).

5. Regarding claim 1, 3 and 17-18, Kelley teaches an organic field effect transistor device (Para. 0012) comprising a substrate (Element 26), a gate insulating film (Element 14) and conductors (Elements 12, 22 and 24), a polymer layer (Element 16) different from the gate insulating film in contact with an organic semiconductor layer (Element 18). The polymer layer

contains a copolymer of methyl methacrylate and divinylbenzene (Col. 6, Lines 30-32 and 53-54). The polymer layer is, for example, 100 Angstroms or 10 nanometers (Col. 5, Lines 14-15).

6. Regarding claims 8-10, the language, term, or phrase "are provided on the substrate in this order", may be directed towards the process of making an organic transistor. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, In re *Brown*, 173 USPQ 685; In re *Luck*, 177 USPQ 523; In re *Fessmann*, 180 USPQ 324; In re *Avery*, 186 USPQ 161; In re *Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re *Marosi* et al., 218 USPQ 289; and particularly In re *Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. However, the claims, as written do limit the structural configuration of the organic transistor to some degree but do not strictly limit the precise orientation between various elements relative to one another. For example, Kelley teaches that the gate electrode, gate insulating film, polymer layer, organic semiconductor and source/drain electrodes are provided on the substrate in order from the substrate upwards (see Fig. 1, for example); the gate electrode, gate insulating film, polymer layer, source/drain electrodes and organic semiconductor are provided on the substrate in order from the substrate upwards (see Fig. 1; Col. 4, Lines 29-31);

the gate electrode, gate insulating film, source/drain electrodes, and polymer layer and the organic semiconductor are provided on the substrate from the substrate upwards (see Fig. 1; Col. 9, Lines 16-22). Furthermore, the Examiner takes the position that the transistor configuration is not critical to the invention. Since applicant has not disclosed any particular advantages of one transistor configuration over another or solves any stated problem uniquely well, it appears that the invention would perform equally well no matter what the transistor configuration is. This is supported by the fact that applicant has claimed several transistor configurations in claims 8-15.

7. Regarding claim 16, the language, term, or phrase "is formed by any one of spin coating, spray coating and dip coating", is directed towards the process of making a polymer layer. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, In re *Brown*, 173 USPQ 685; In re *Luck*, 177 USPQ 523; In re *Fessmann*, 180 USPQ 324; In re *Avery*, 186 USPQ 161; In re *Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re *Marosi* et al., 218 USPQ 289; and particularly In re *Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. As such, the language "is formed by any one of spin coating, spray coating and dip coating" only requires a polymer layer, which does not distinguish the invention from

Kelley, who teaches the structure as claimed. Nevertheless, Kelley teaches that the polymer layer can be formed by spin coating, spray coating and dip coating (Col. 9, Lines 5-8).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley (`676) in view of Ittmann (`901).

Kelley teaches the polymer layer of methyl methacrylate (A) and divinylbenzene (B) as shown above, which can be formed by casting methods, such as a spin coating process (Col. 9, Lines 5-15), but does not suggest that the monomer ratio be from 1:0.001 to 1:0.04.

Ittmann teaches using methyl methacrylate (A) with a cross-linker comonomer of divinylbenzene (B) for example, in a, for example 1:0.02 ratio (Col. 4, Lines 11-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a, for example, 1:0.02 ratio between (A) and (B) in order to keep the viscosity low (Col. 3, Lines 38-40; Col. 4, Lines 52-56, for example) in order to produce a copolymer which has excellent casting properties in order to form the thin and evenly formed polymer layer required by Kelley (Kelley Col. 5, Lines 10-18; Col. 9, Lines 5-28). It has been held that where the general

conditions of a claim are disclosed in prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley (`676) in view of Choi (`487) in view of Sirringhaus (`394).

Kelley teaches that the organic semiconductor device has the polymer layer between the organic semiconductor and gate insulating film and being in contact with each of the layers (see Fig. 1, for example). However, Kelley does not teach that the surface roughness of the gate insulator is RMS 5nm or less.

Choi teaches gate insulator films with, for example, RMS roughness less than 3 Angstroms or less (Para. 0065). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a gate insulating film with an RMS surface roughness of 3 Anstroms or less. One would have been motivated to do so since Choi teaches that these gate insulator layers have excellent performance characteristics in organic transistors (Para. 0065). More specifically, Sirringhaus teaches that very smooth gate insulator layers formed in contact with polymer alignment layers in order to maintain a smooth interface for improved organic transistor performance (Col. 7, Lines 38-47).

11. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley (`676) in view of Nagayama (`017).

The language, term, or phrase "are provided on the substrate in this order", may be directed towards the process of making an organic transistor. It is well settled that "product by

process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, In re *Brown*, 173 USPQ 685; In re *Luck*, 177 USPQ 523; In re *Fessmann*, 180 USPQ 324; In re *Avery*, 186 USPQ 161; In re *Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re *Marosi* et al., 218 USPQ 289; and particularly In re *Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. However, the claims, as written do limit the structural configuration of the organic transistor to some degree but do not strictly limit the precise orientation between various elements relative to one another. For example, Kelley teaches a conventional bottom gate transistor structure with the polymer layer in contact with organic semiconductor layer (Fig. 1), but does not teach the conventional vertical transistor structure with the source/drain electrodes each on opposite sides of the organic semiconductor layer.

Nagayama teaches the conventional organic transistor structures, including top gate (Fig. 17, for example), bottom gate (Figs. 1-2), static induction (Fig. 8), and the vertical configuration with the source/drain electrodes each on opposite sides of the organic semiconductor layer (Figs. 10 and 18; Para. 0082, 0130). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the conventional vertical configuration with the source/drain electrodes each on opposite sides of the organic semiconductor layer since

Nagayama teaches that the vertical configuration is functionally equivalent to other conventional organic transistor configurations.

Furthermore, the Examiner takes the position that the transistor configuration is not critical to the invention. Since applicant has not disclosed any particular advantages of one transistor configuration over another or solves any stated problem uniquely well, it appears that the invention would perform equally well no matter what the transistor configuration is. This is supported by the fact that applicant has claimed several transistor configurations in claims 8-15.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley (`676) in view of Dimitrakopoulos (`873).

The language, term, or phrase "are provided on the substrate in this order", may be directed towards the process of making an organic transistor. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, In re *Brown*, 173 USPQ 685; In re *Luck*, 177 USPQ 523; In re *Fessmann*, 180 USPQ 324; In re *Avery*, 186 USPQ 161; In re *Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re *Marosi* et al., 218 USPQ 289; and particularly In re *Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference.

However, the claims, as written do limit the structural configuration of the organic transistor to some degree but do not strictly limit the precise orientation between various elements relative to one another. For example, Kelley teaches several conventional bottom gate configurations for forming organic transistors wherein the polymer layer (used for increasing organic transistor device performance as described in Kelley Col. 2, Lines 12-18, for example) is formed in contact with the organic semiconductor layer, but does not teach the conventional top gate configurations.

Dimitrakopoulos teaches both conventional top gate and bottom gate configurations of organic devices with a polymer layer used for increasing organic transistor device performance (Para. 0047, for example), with a substrate (Element 10), source/drain electrodes (Element 20) formed on the substrate, polymer layer (Element 18, 22) formed on the substrate, an organic semiconductor layer (Element 16), a gate insulating film (Element 14), and a gate electrode (Element 12) formed in order on the substrate from the bottom upwards (Fig. 4, for example). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the conventional top gate configuration in place of the conventional bottom gate configuration since Dimitrakopoulos teaches that they are functionally equivalent. Dimitrakopoulos further teaches that the polymer layer acts to orient the organic semiconductor material on improves the electrical device performance of the organic semiconductor layer (Para. 0047, 0064-0066).

Furthermore, the Examiner takes the position that the transistor configuration is not critical to the invention. Since applicant has not disclosed any particular advantages of one transistor configuration over another or solves any stated problem uniquely well, it appears that

the invention would perform equally well no matter what the transistor configuration is. This is supported by the fact that applicant has claimed several transistor configurations in claims 8-15.

13. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley ('676) in view of Sirringhaus ('394).

The language, term, or phrase "are provided on the substrate in this order", may be directed towards the process of making an organic transistor. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, In re *Brown*, 173 USPQ 685; In re *Luck*, 177 USPQ 523; In re *Fessmann*, 180 USPQ 324; In re *Avery*, 186 USPQ 161; In re *Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re *Marosi* et al., 218 USPQ 289; and particularly In re *Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. However, the claims, as written do limit the structural configuration of the organic transistor to some degree but do not strictly limit the precise orientation between various elements relative to one another. For example, Kelley teaches several conventional bottom gate configurations for forming organic transistors wherein the polymer layer (used for increasing organic transistor device performance as described in Kelley Col. 2, Lines 12-18, for example) is formed in contact

with the organic semiconductor layer, but does not teach the conventional top gate configurations.

Sirringhaus teaches both conventional top gate and bottom gate configurations of organic devices with a polymer layer used for increasing organic transistor device performance (Fig. 9b and 9c, for example, showing bottom gate and Figs. 1 and 9a, for example, showing top gate). For example, Sirringhaus teaches a substrate, polymer alignment layer formed on the substrate, source/drain electrodes formed on the polymer layer, an organic semiconductor layer formed on the source/drain electrodes, a gate insulator formed on the organic semiconductor and a gate electrode formed on the gate insulator (Fig. 1). In another top gate example, Sirringhaus teaches a substrate, a polymer alignment layer formed on the substrate, an organic semiconductor on the polymer layer, source/drain electrodes on the organic semiconductor, a gate insulator on the source/drain electrodes, and a gate electrode and the gate insulator (Fig. 9a). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the conventional top gate configuration in place of the conventional bottom gate configuration since Sirringhaus teaches that they are functionally equivalent (Col. 7, Lines 48-53). The configuration of Fig. 1 is useful for improving the charge transport properties of the organic semiconductor layer formed on the polymer alignment layer (Col. 5, Lines 31-32). Sirringhaus also teaches that the configuration taught in Fig. 9a is advantageous since it allows for the improved alignment near the source/drain electrodes and facilitates charge injection (Col. 11, Lines 2-6).

Furthermore, the Examiner takes the position that the transistor configuration is not critical to the invention. Since applicant has not disclosed any particular advantages of one

transistor configuration over another or solves any stated problem uniquely well, it appears that the invention would perform equally well no matter what the transistor configuration is. This is supported by the fact that applicant has claimed several transistor configurations in claims 8-15.

14. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kelley (`676) in view of Sirringhaus (`394) in view of Nagayama (`017).

The language, term, or phrase "are provided on the substrate in this order", may be directed towards the process of making an organic transistor. It is well settled that "product by process" limitations in claims drawn to structure are directed to the product, per se, no matter how actually made. In re *Hirao*, 190 USPQ 15 at 17 (footnote 3). See also, In re *Brown*, 173 USPQ 685; In re *Luck*, 177 USPQ 523; In re *Fessmann*, 180 USPQ 324; In re *Avery*, 186 USPQ 161; In re *Wethheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re *Marosi* et al., 218 USPQ 289; and particularly In re *Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or otherwise. The above case law further makes clear that applicant has the burden of showing that the method language necessarily produces a structural difference. However, the claims, as written do limit the structural configuration of the organic transistor to some degree but do not strictly limit the precise orientation between various elements relative to one another. For example, Kelley teaches several conventional bottom gate configurations for forming organic transistors wherein the polymer layer (used for increasing organic transistor

device performance as described in Kelley Col. 2, Lines 12-18, for example) is formed in contact with the organic semiconductor layer, but does not teach the conventional top gate configurations.

Sirringhaus teaches both conventional top gate and bottom gate configurations of organic devices with a polymer layer used for increasing organic transistor device performance (Fig. 9b and 9c, for example, showing bottom gate and Figs. 1 and 9a, for example, showing top gate). For example, Sirringhaus teaches a substrate, polymer alignment layer formed on the substrate, source/drain electrodes formed on the polymer layer, an organic semiconductor layer formed on the source/drain electrodes, a gate insulator formed on the organic semiconductor and a gate electrode formed on the gate insulator (Fig. 1). In another top gate example, Sirringhaus teaches a substrate, a polymer alignment layer formed on the substrate, an organic semiconductor on the polymer layer, source/drain electrodes on the organic semiconductor, a gate insulator on the source/drain electrodes, and a gate electrode and the gate insulator (Fig. 9a). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the conventional top gate configuration in place of the conventional bottom gate configuration since Sirringhaus teaches that they are functionally equivalent (Col. 7, Lines 48-53). The configuration of Fig. 1 is useful for improving the charge transport properties of the organic semiconductor layer formed on the polymer alignment layer (Col. 5, Lines 31-32). Sirringhaus also teaches that the configuration taught in Fig. 9a is advantageous since it allows for the improved alignment near the source/drain electrodes and facilitates charge injection (Col. 11, Lines 2-6). While Kelley and Sirringhaus each teach conventional transistor structures with the polymer layer in contact with organic semiconductor layer (see Figures), neither teaches the

conventional vertical transistor structure with the source/drain electrodes each on opposite sides of the organic semiconductor layer.

Nagayama teaches the conventional organic transistor structures, including top gate (Fig. 17, for example), bottom gate (Figs. 1-2), static induction (Fig. 8), and the vertical configuration with the source/drain electrodes each on opposite sides of the organic semiconductor layer (Figs. 10 and 18; Para. 0082, 0130). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the conventional vertical configuration with the source/drain electrodes each on opposite sides of the organic semiconductor layer since Nagayama teaches that the vertical configuration is functionally equivalent to other conventional organic transistor configurations.

Furthermore, the Examiner takes the position that the transistor configuration is not critical to the invention. Since applicant has not disclosed any particular advantages of one transistor configuration over another or solves any stated problem uniquely well, it appears that the invention would perform equally well no matter what the transistor configuration is. This is supported by the fact that applicant has claimed several transistor configurations in claims 8-15.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

a. Kelley (`359) teaches a polymer layer on the gate insulator of an organic transistor (OTFT) which improves the performance of the organic semiconductor;

b. Jackson (`572) teaches a conventional vertical configuration for OTFT;

c. Veres (`945) teaches several conventional top gate and bottom gate configurations for OTFT, and polymer layers on gate insulators to improve performance characteristics.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Such whose telephone number is (571) 272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew W. Such
Examiner
Art Unit 2891

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

MWS
9/21/07